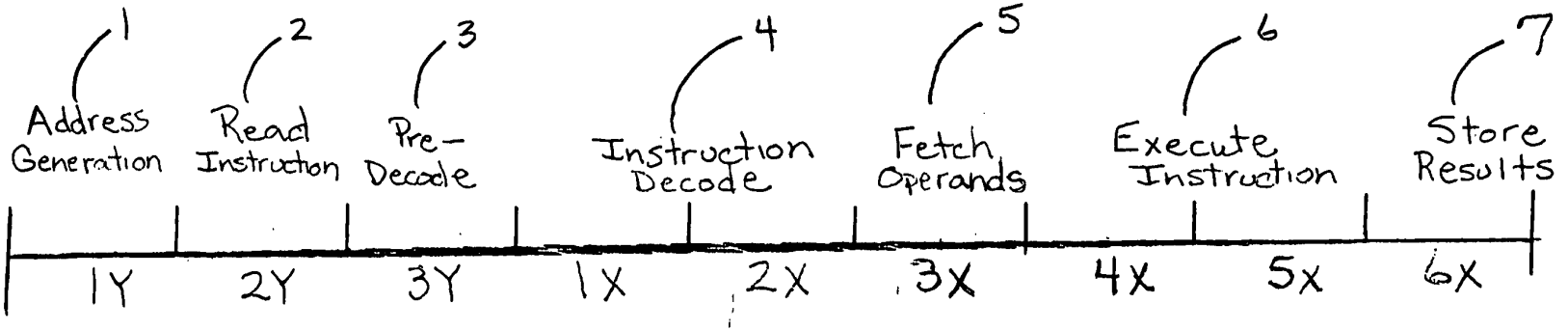


Figure 1

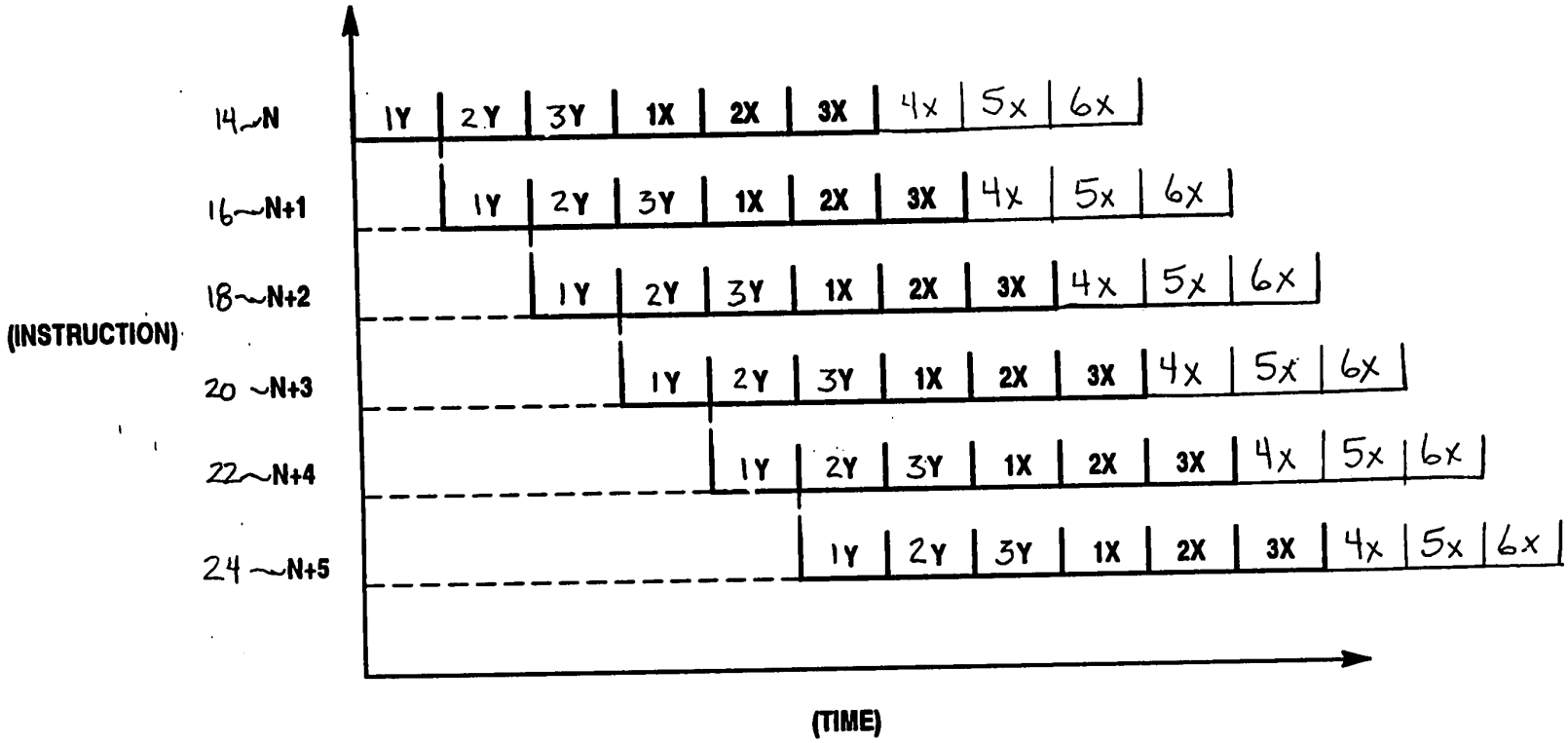


Figure 2

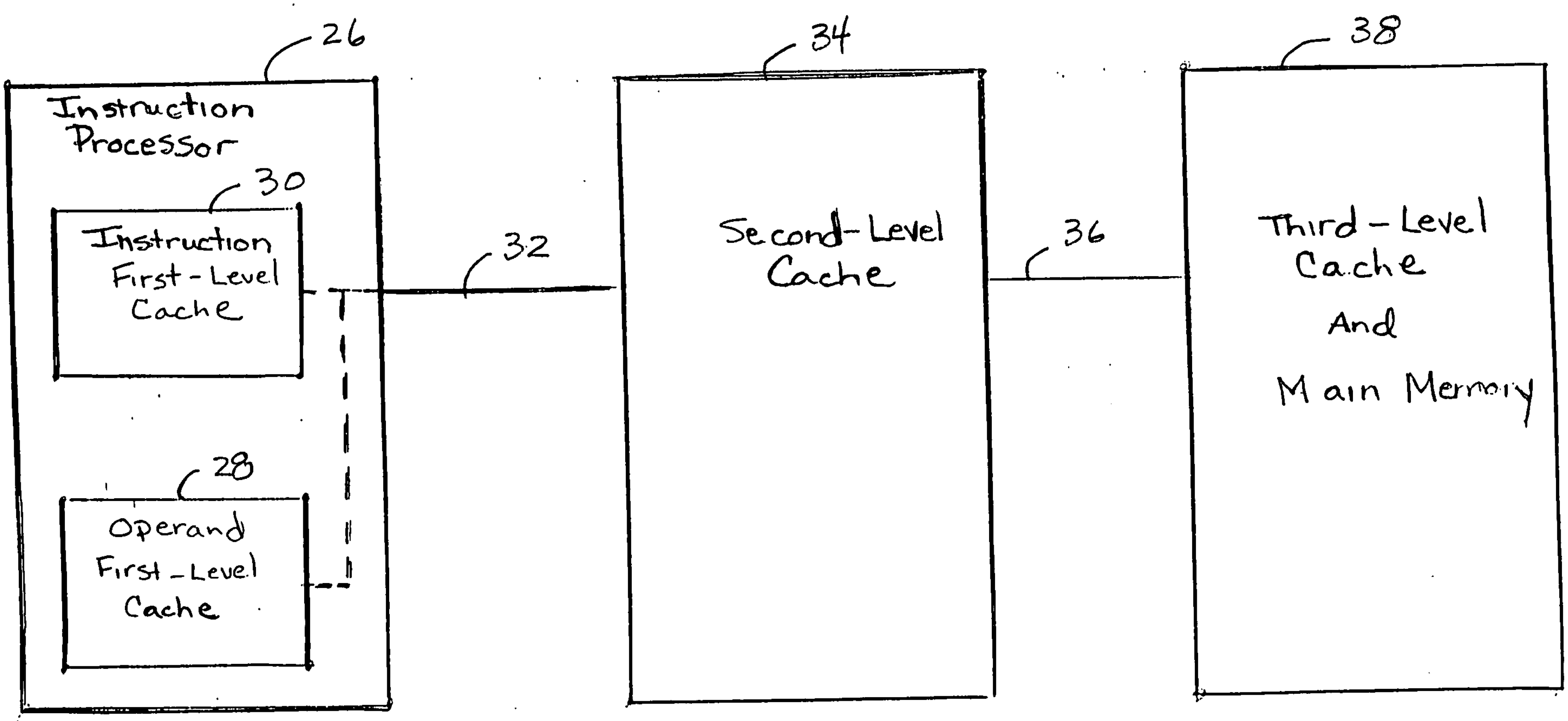

26
Instruction
Processor
30
Instruction
First-Level
Cache
28
Operand
First-Level
Cache
32
34
Second-Level
Cache
36
38
Third-Level
Cache
And
Main Memory

Figure 3

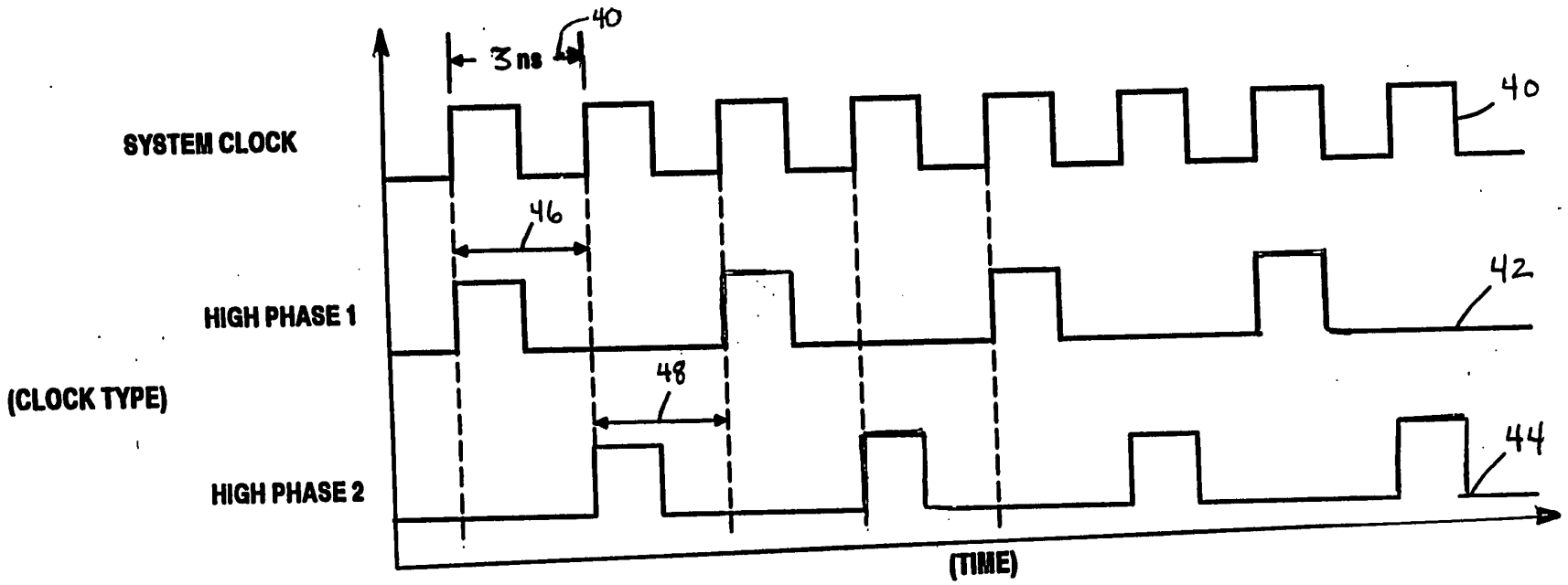


Figure 4

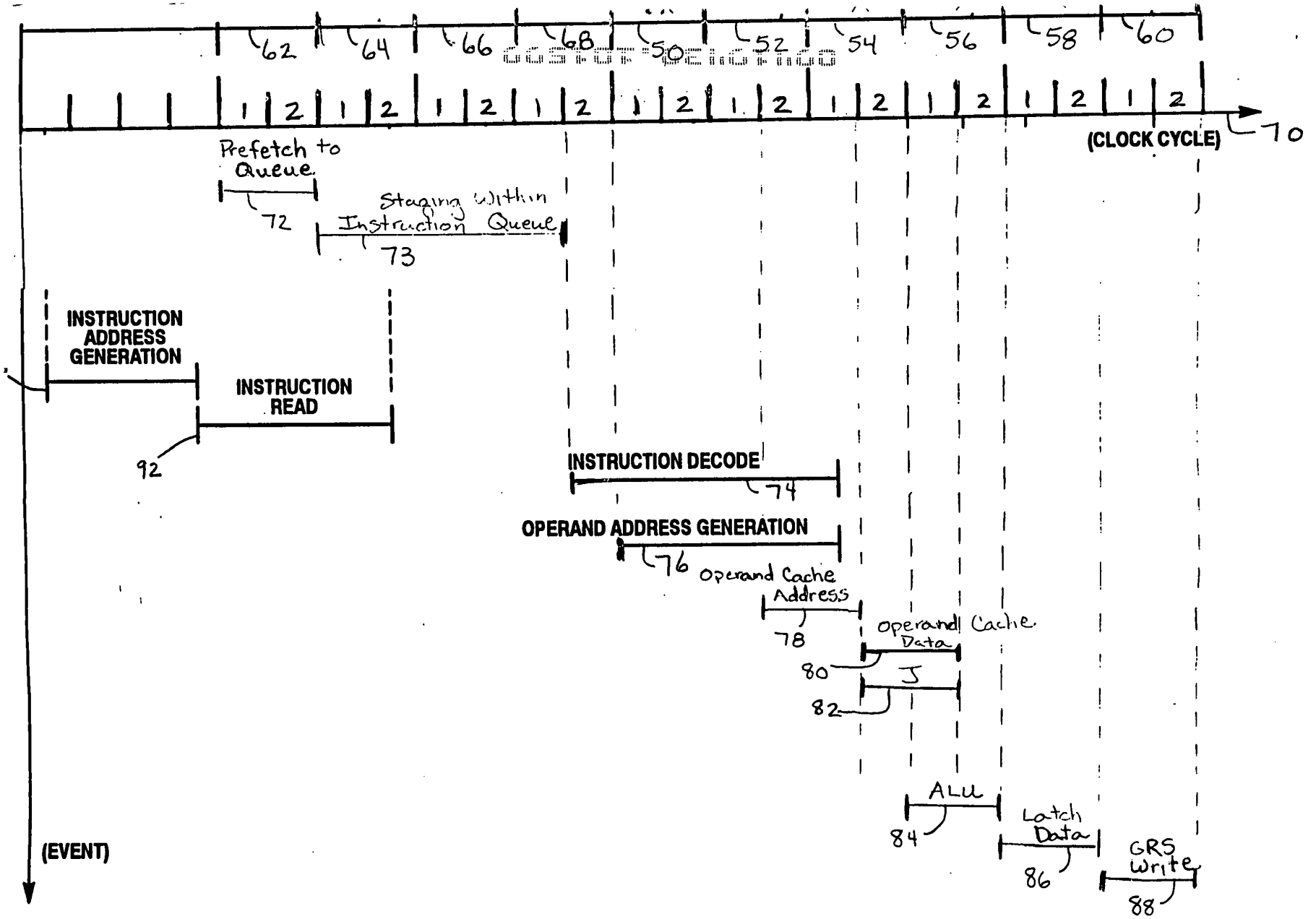

62
64
66
68
50
52
54
56
58
60
1
2
(CLOCK CYCLE)
70
Prefetch to Queue
72
Staging Within Instruction Queue
73
INSTRUCTION ADDRESS GENERATION
INSTRUCTION READ
92
INSTRUCTION DECODE
74
OPERAND ADDRESS GENERATION
76
Operand Cache Address
78
Operand Cache Data
80
J
82
ALU
84
Latch Data
86
GRS Write
88
(EVENT)

Figure 5

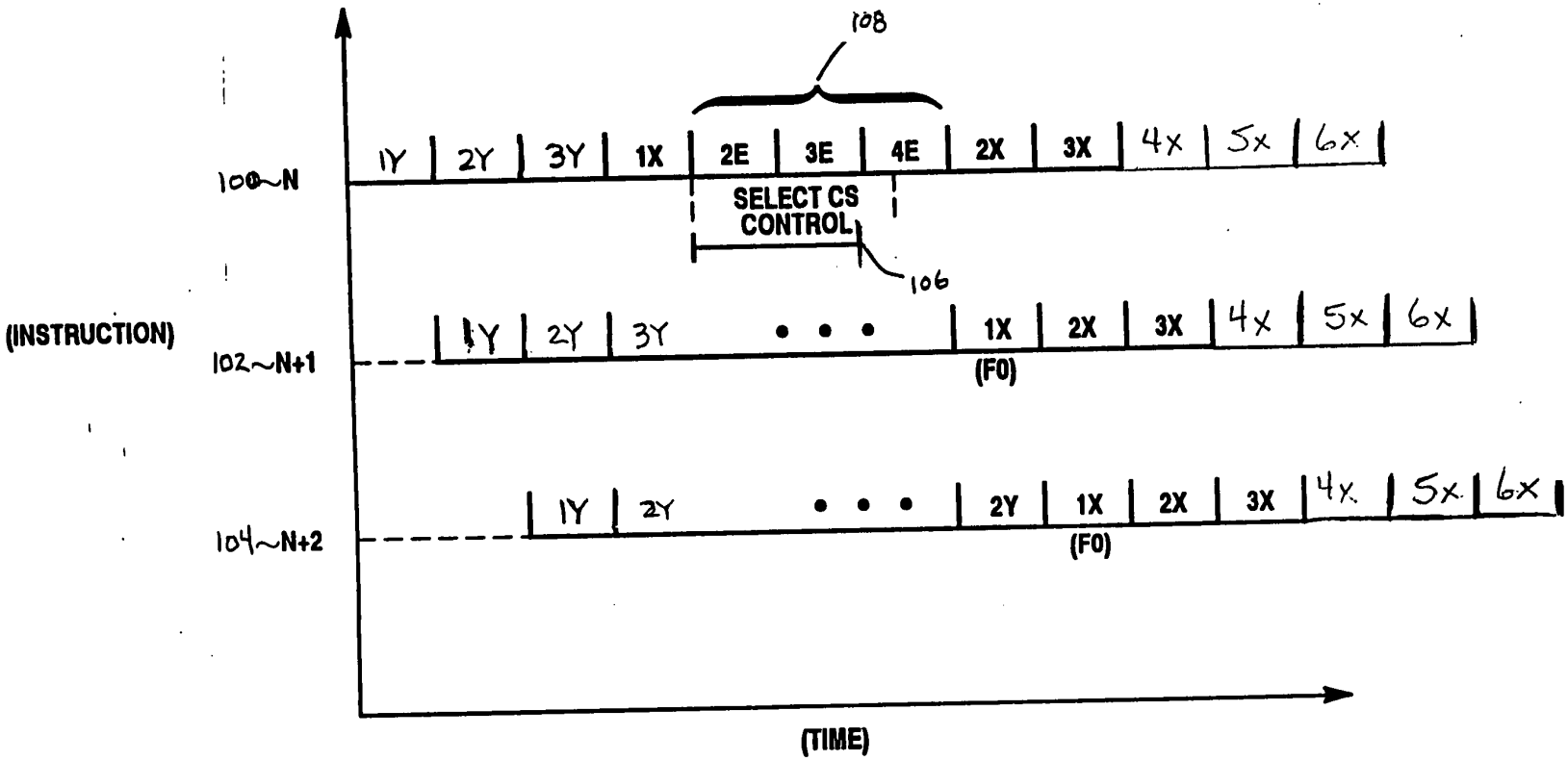


Figure 6

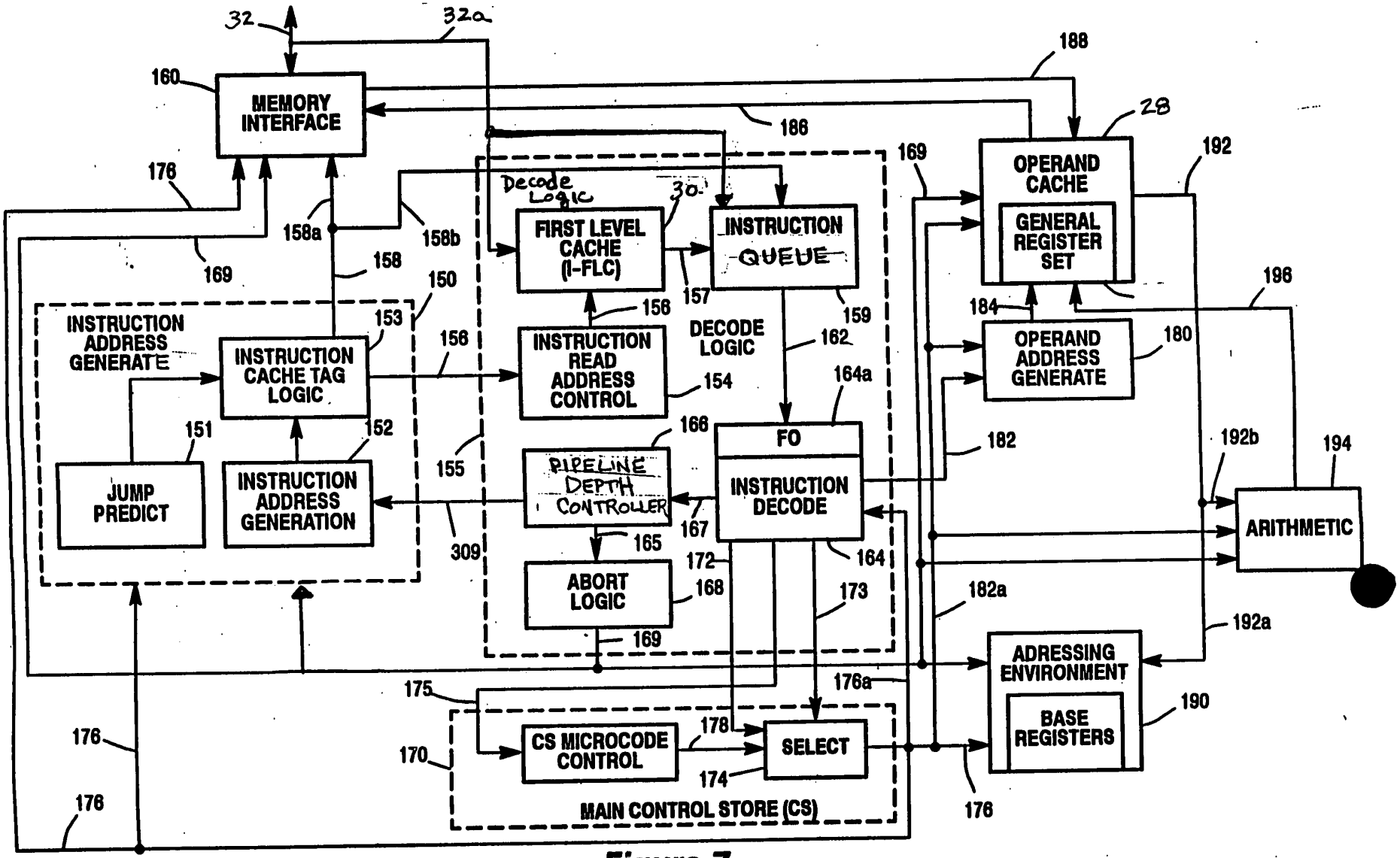

To Second-Level Cache
32
32a
160
MEMORY INTERFACE
188
186
28
176
Decode Logic
30
FIRST LEVEL CACHE (I-FLC)
INSTRUCTION QUEUE
169
OPERAND CACHE
GENERAL REGISTER SET
192
158a
158b
158
169
150
196
INSTRUCTION ADDRESS GENERATE
153
INSTRUCTION CACHE TAG LOGIC
156
157
159
184
INSTRUCTION READ ADDRESS CONTROL
DECODE LOGIC
162
OPERAND ADDRESS GENERATE
180
154
164a
151
152
166
FO
182
192b
194
JUMP PREDICT
INSTRUCTION ADDRESS GENERATION
155
PIPELINE DEPTH CONTROLLER
INSTRUCTION DECODE
ARITHMETIC
309
167
165
164
172
ABORT LOGIC
168
173
182a
192a
169
ADRESSING ENVIRONMENT
176a
175
BASE REGISTERS
190
176
CS MICROCODE CONTROL
178
SELECT
170
174
MAIN CONTROL STORE (CS)
176
176

Figure 7

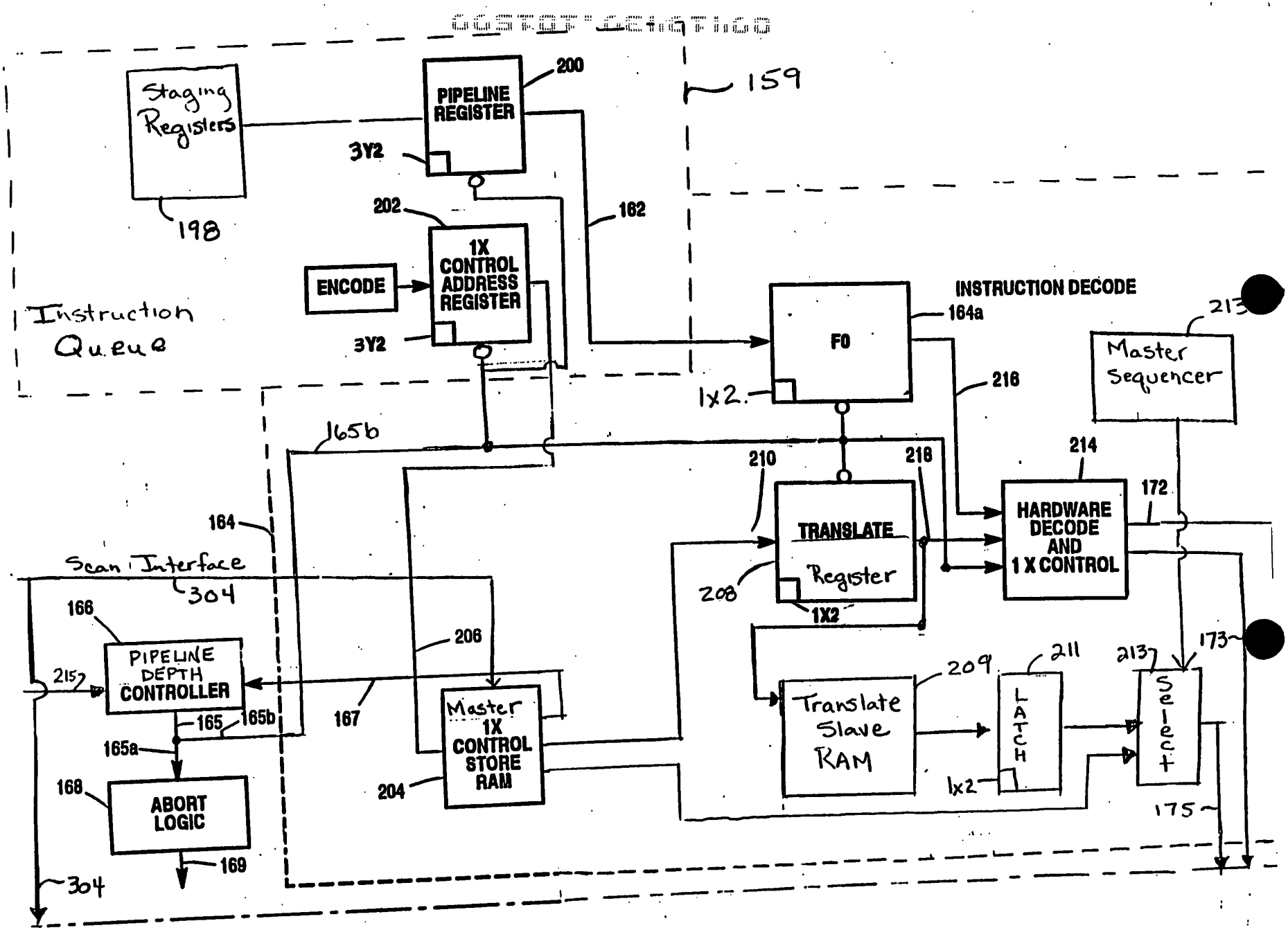

Staging Registers
198
PIPELINE REGISTER
200
3Y2
159
202
1X CONTROL ADDRESS REGISTER
ENCODE
3Y2
162
Instruction Queue
INSTRUCTION DECODE
F0
164a
1x2
216
213
Master Sequencer
165b
210
218
214
172
TRANSLATE Register
1X2
208
HARDWARE DECODE AND 1 X CONTROL
164
Scan Interface
304
166
PIPELINE DEPTH CONTROLLER
215
206
167
165
165b
165a
Master 1X CONTROL STORE RAM
204
209
211
213
173
Translate Slave RAM
LATCH
1x2
Select
175
168
ABORT LOGIC
169
304

Figure 8A

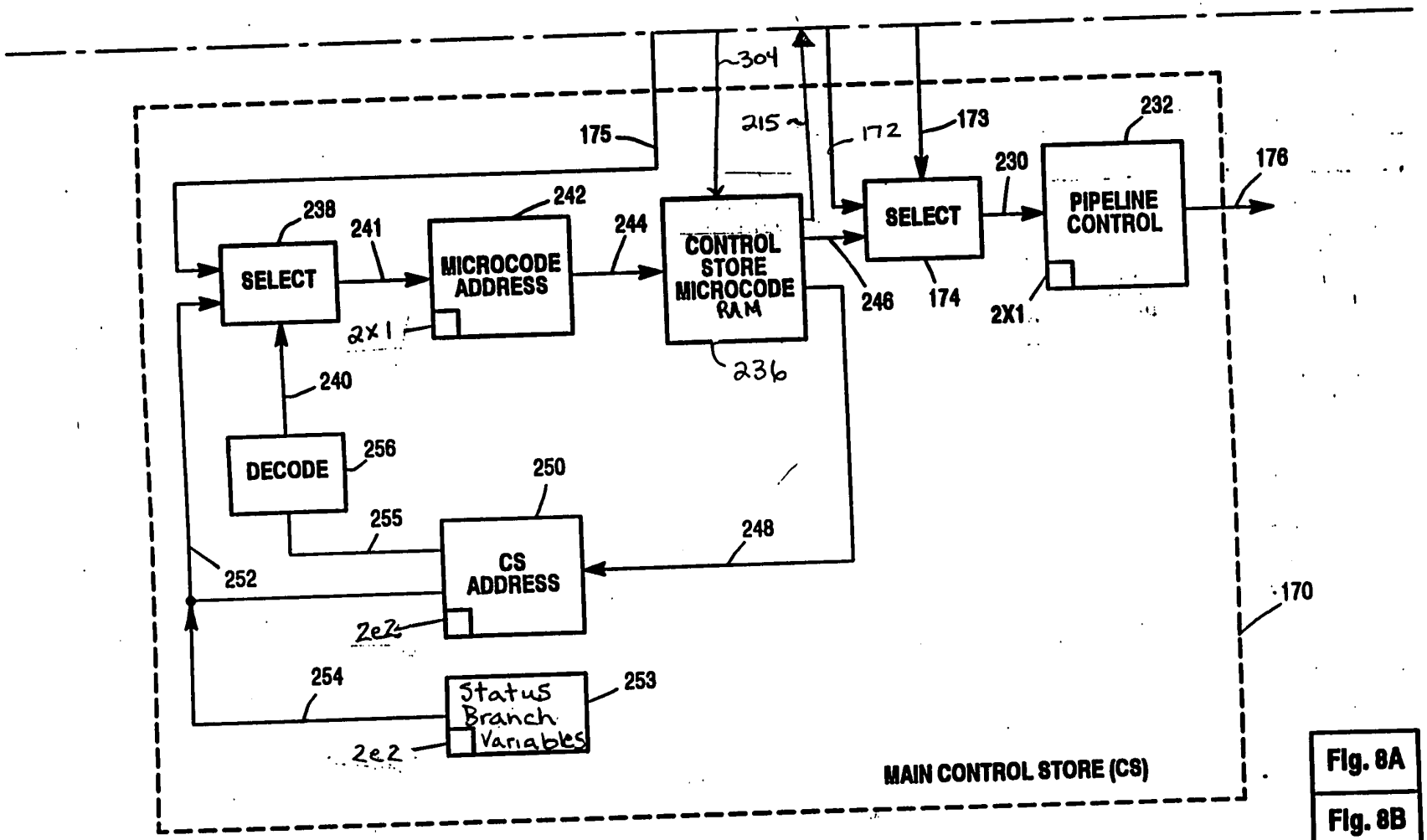


Fig. 8A
Fig. 8B

Figure 8B

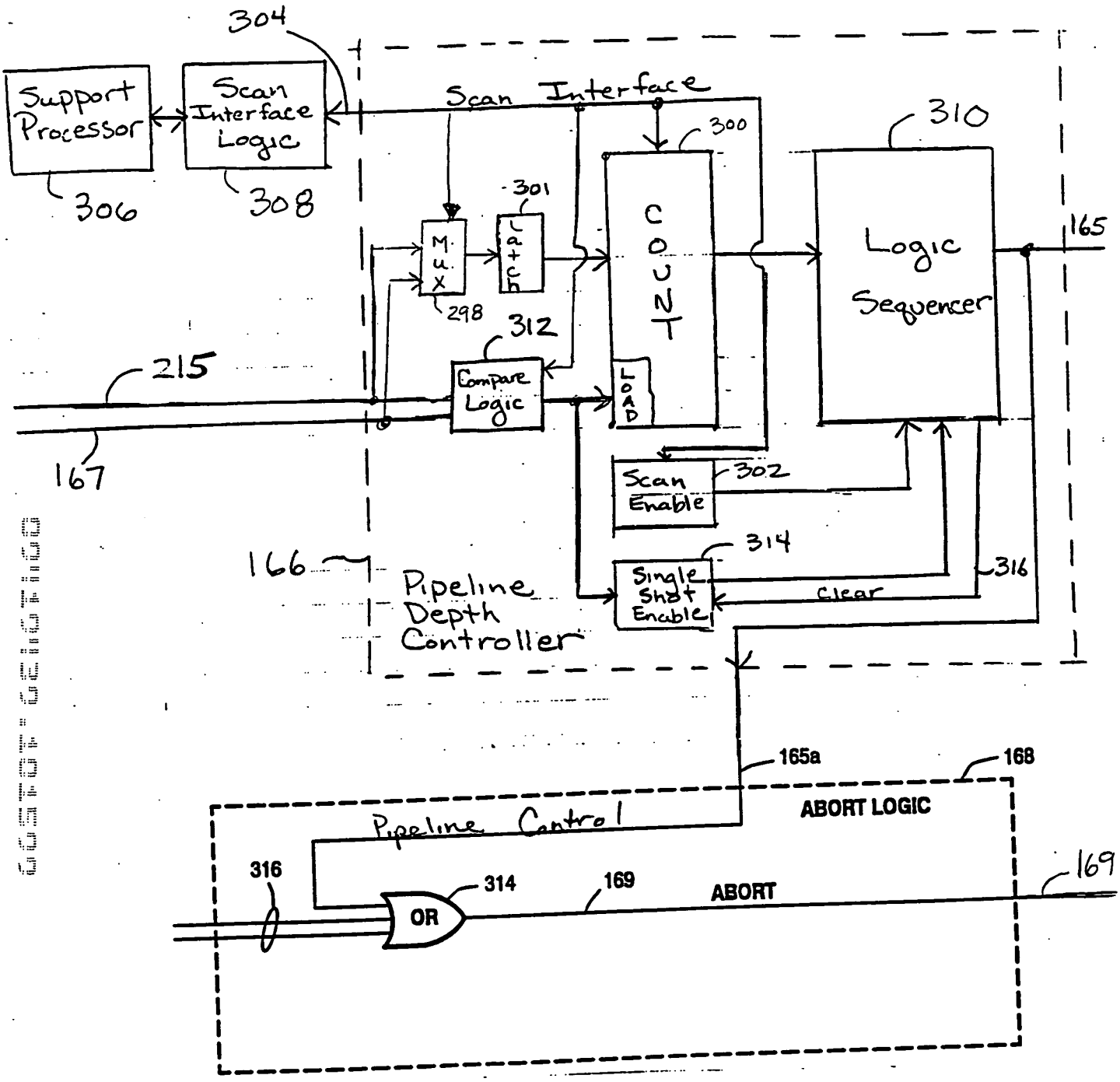
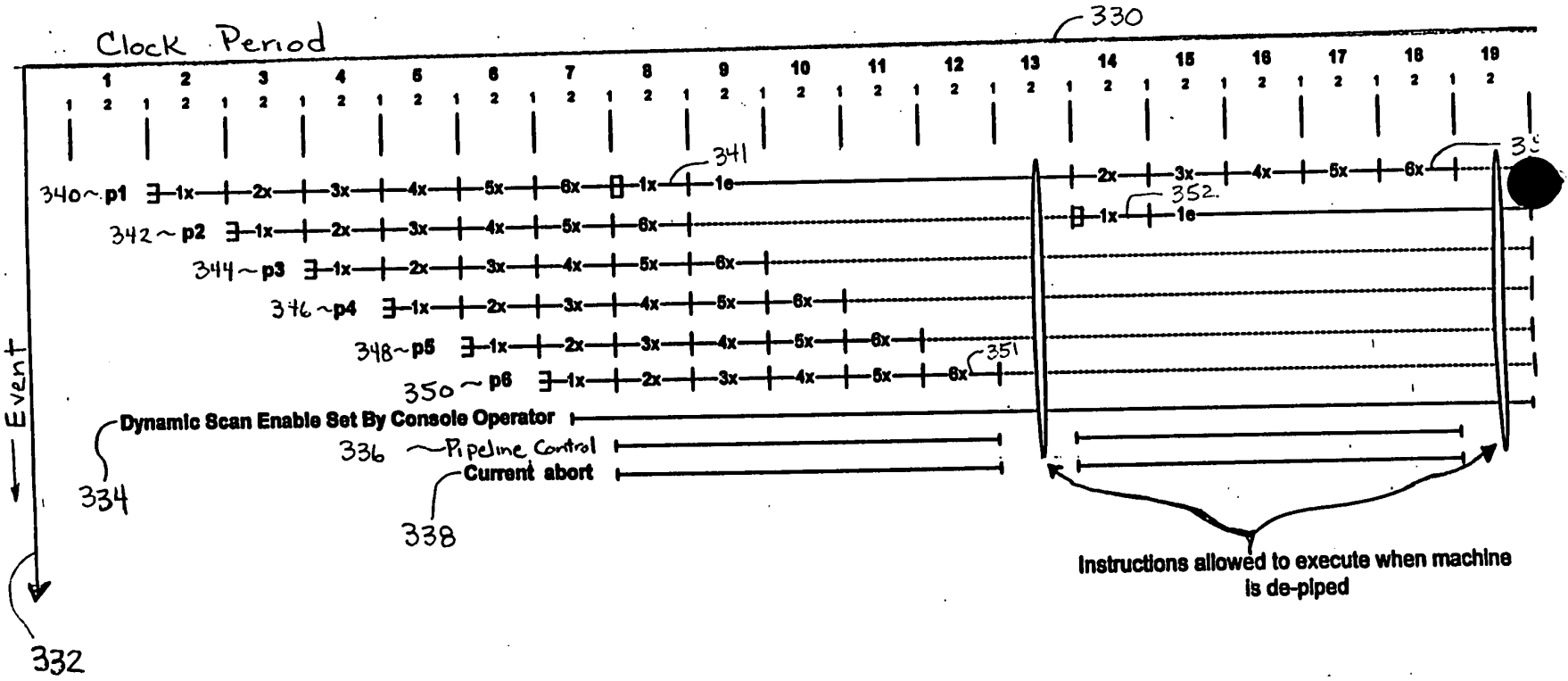
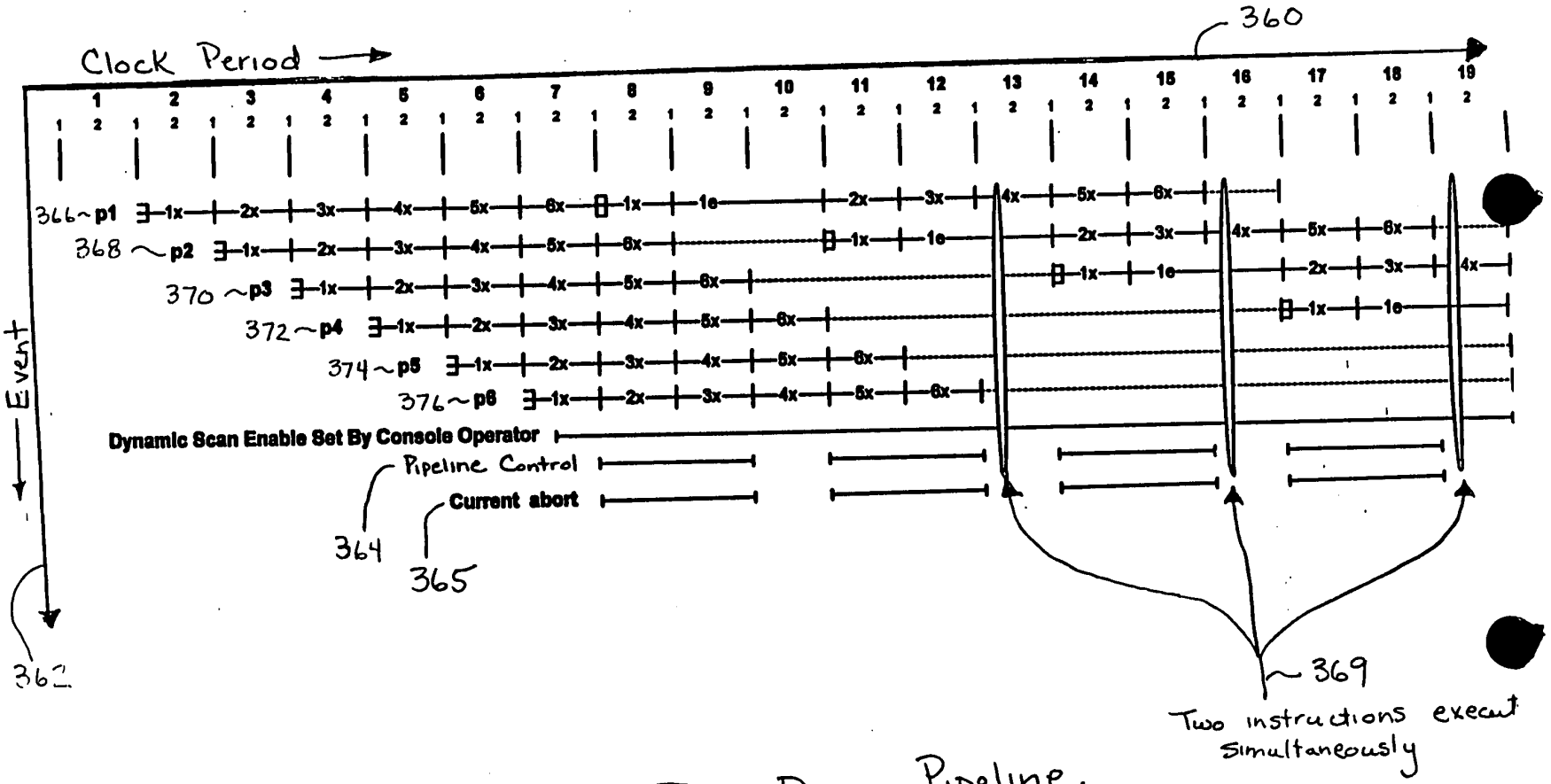

304
Support Processor
Scan Interface Logic
Scan Interface
306
308
300
310
301
Latch
Mux
298
COUNT
Logic Sequencer
165
312
215
Compare Logic
LOAD
167
Scan Enable
302
166
314
Pipeline Depth Controller
Single Shot Enable
316
Clear
165a
168
ABORT LOGIC
Pipeline Control
316
314
169
ABORT
OR

Figure 9



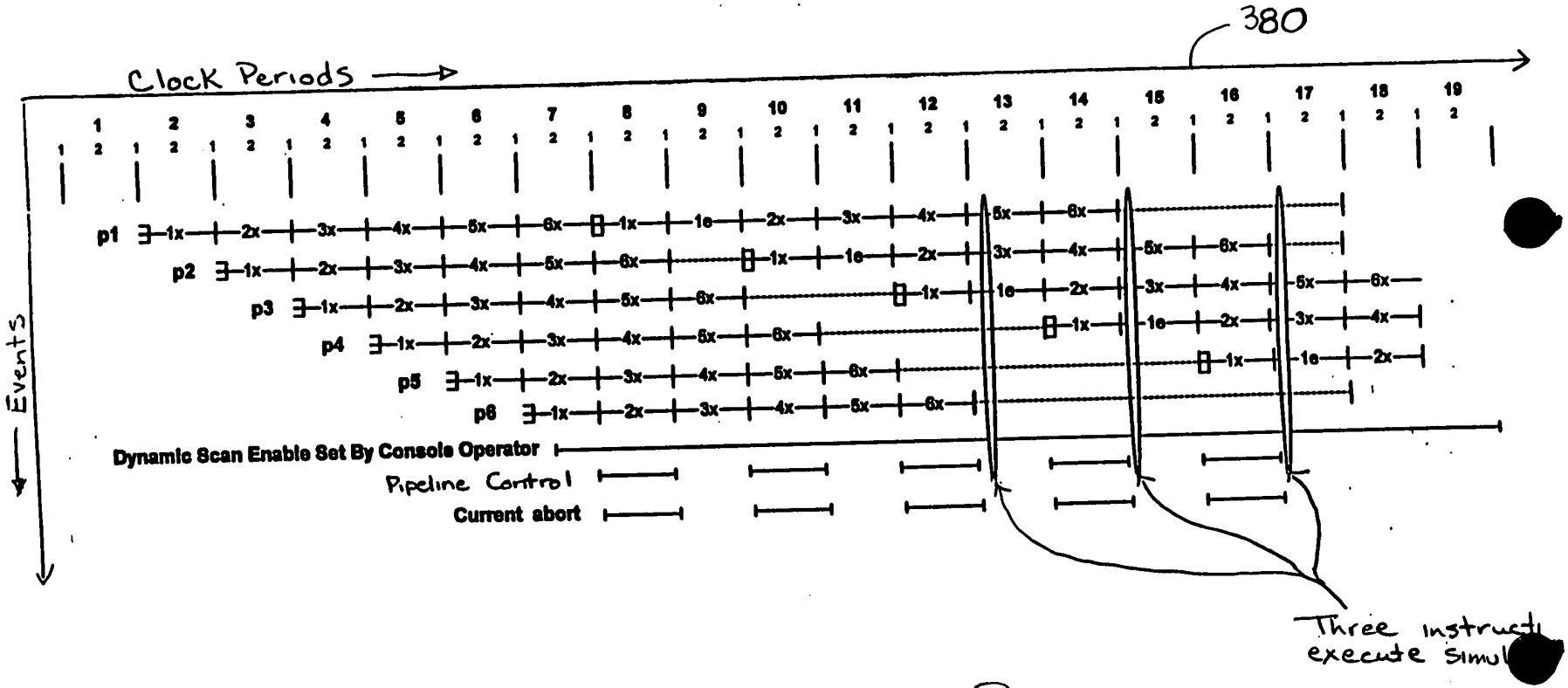
One-Deep Pipeline

Figure 10



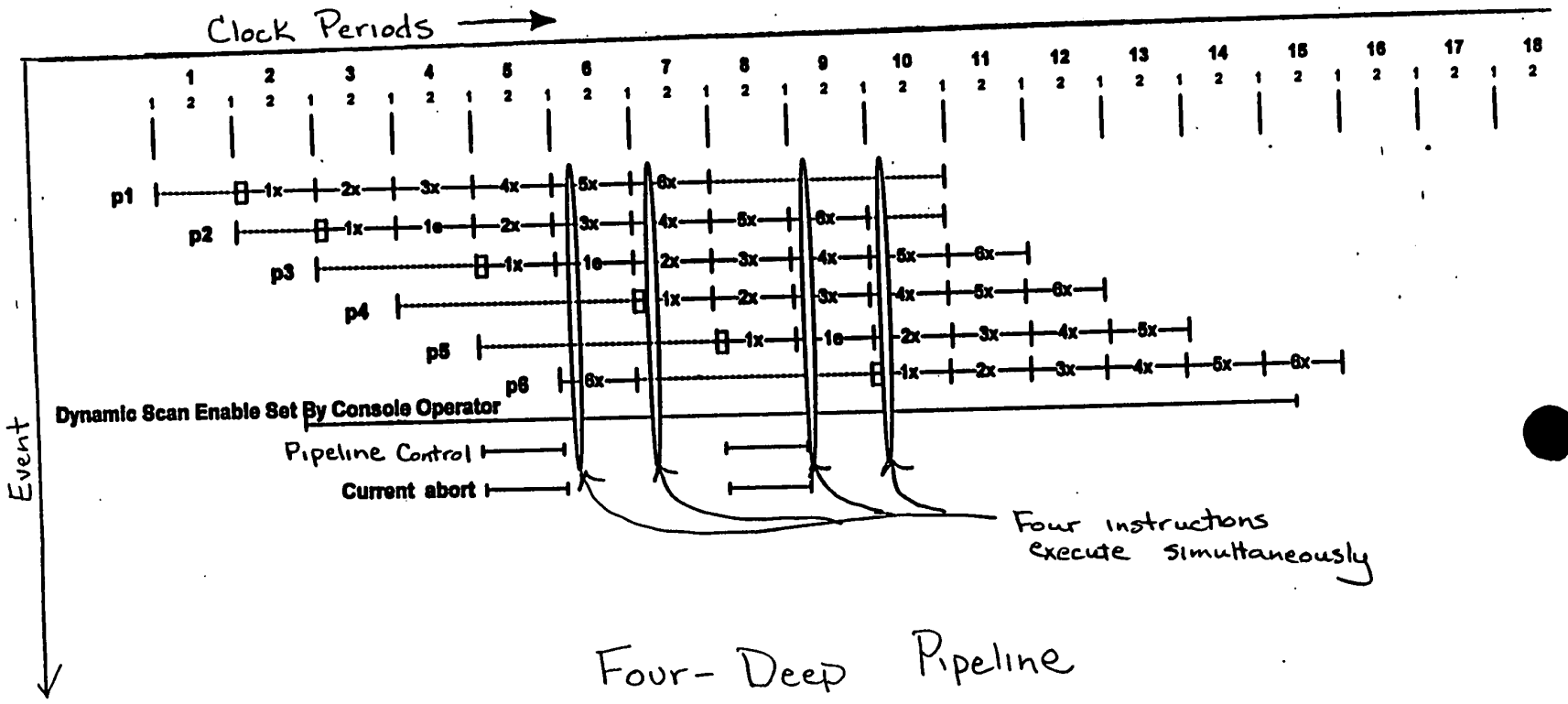
Two-Deep Pipeline

Figure 11



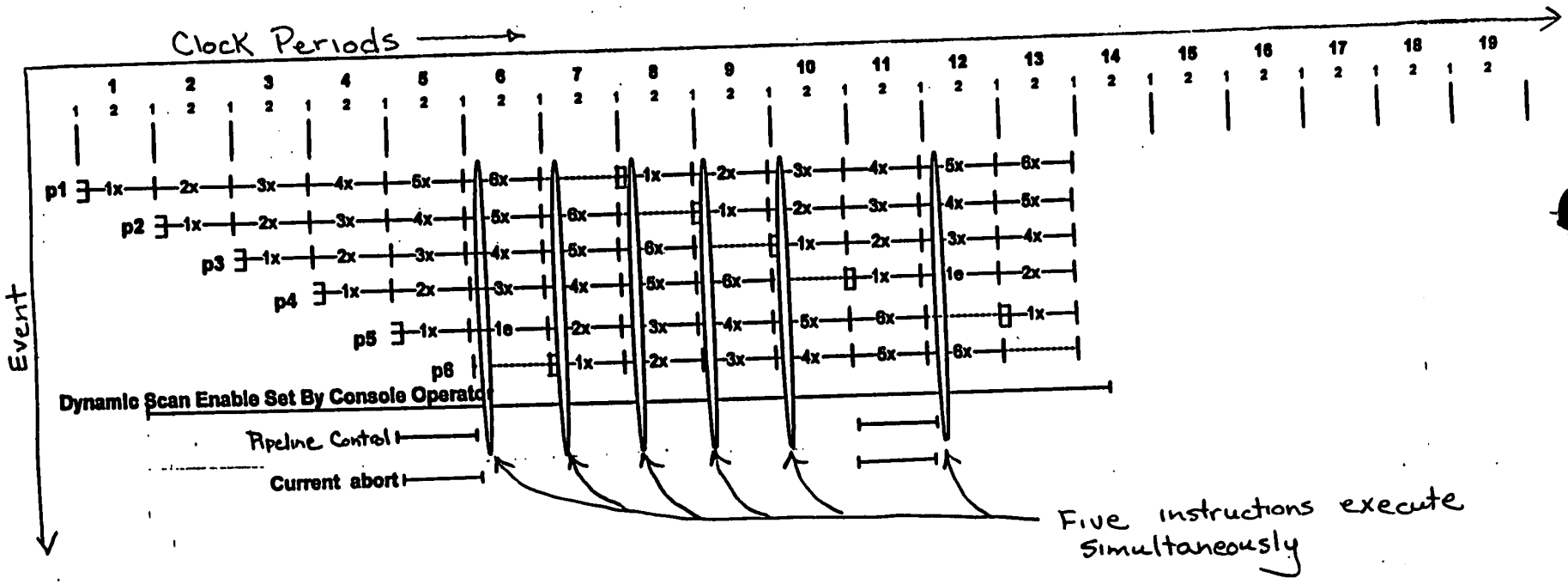
Three-Deep Pipeline

Figure 12



Four- Deep Pipeline

Figure 13



Five- Deep Pipeline

Figure 14

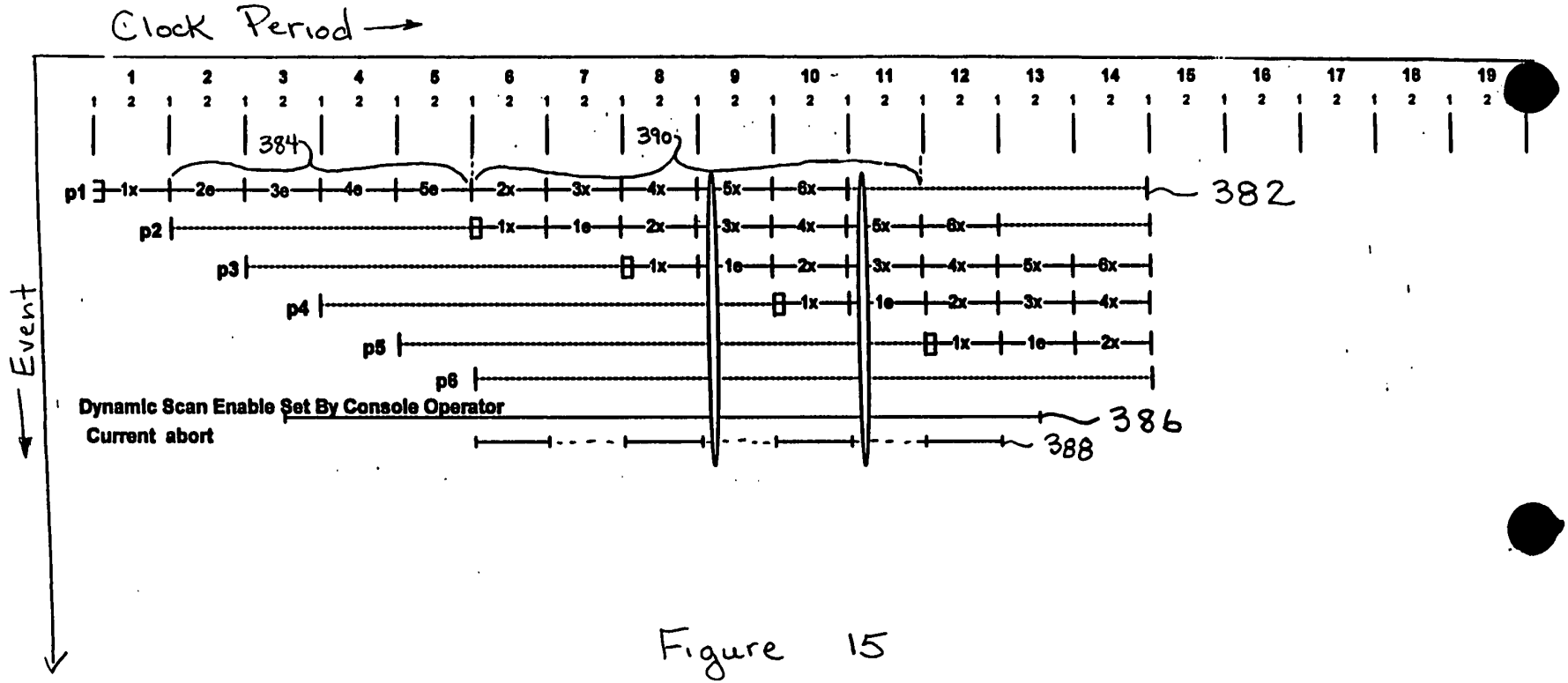

Clock Period
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
384
390
p1 1x 2e 3e 4e 5e 2x 3x 4x 5x 6x
382
p2 1x 1e 2x 3x 4x 5x 6x
p3 1x 1e 2x 3x 4x 5x 6x
p4 1x 1e 2x 3x 4x
p5 1x 1e 2x
p6
Dynamic Scan Enable Set By Console Operator
386
Current abort
388
Event

Figure 15

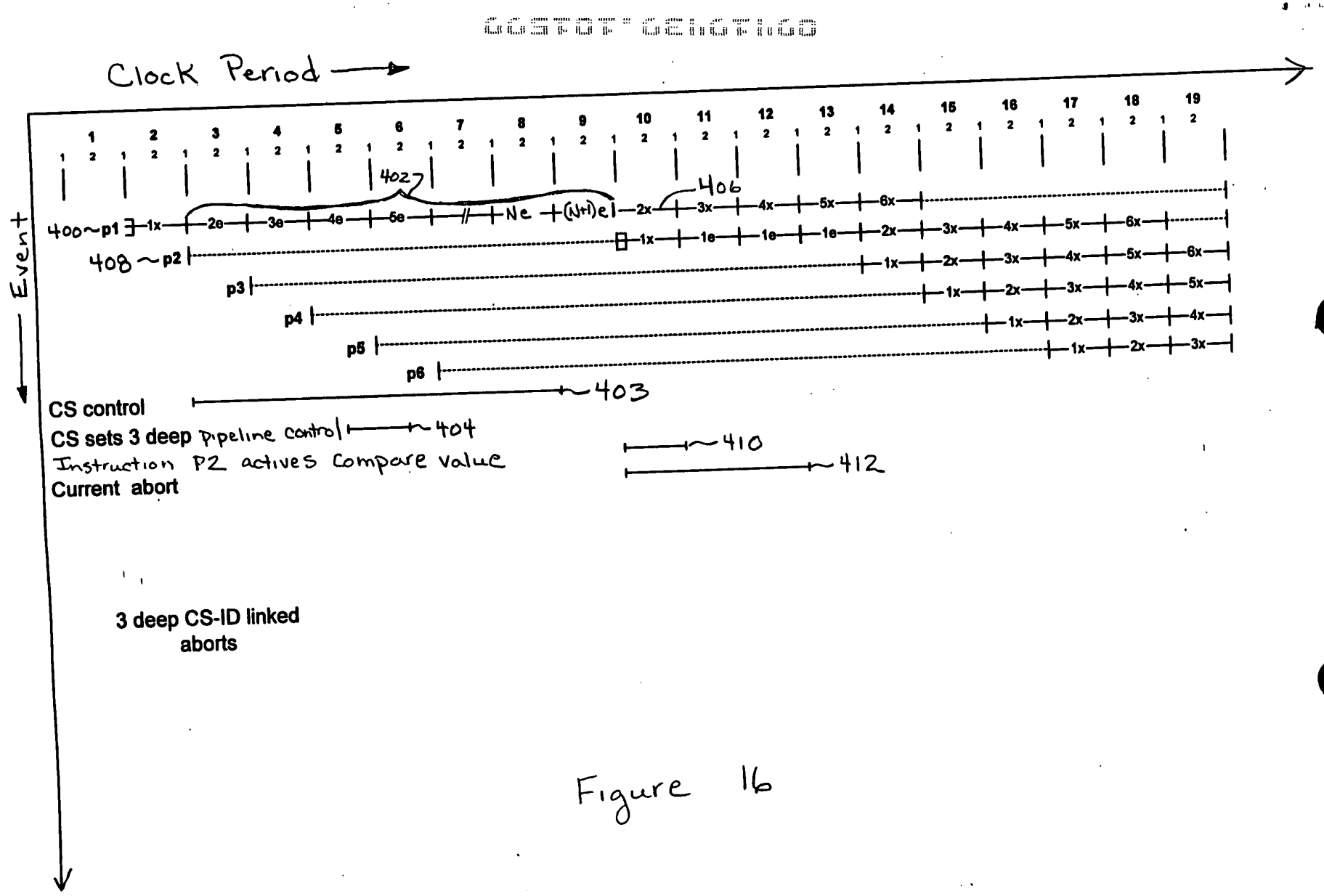

Clock Period
Event
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
402
406
400~p1
408~p2
p3
p4
p5
p6
1x 2e 3e 4e 5e Ne (Nri)e 2x 3x 4x 5x 6x
1x 1e 1e 1e 2x 3x 4x 5x 6x
1x 2x 3x 4x 5x 6x
1x 2x 3x 4x 5x
1x 2x 3x 4x
1x 2x 3x
403
CS control
CS sets 3 deep pipeline control
404
Instruction P2 actives Compare value
410
Current abort
412
3 deep CS-ID linked aborts

Figure 16

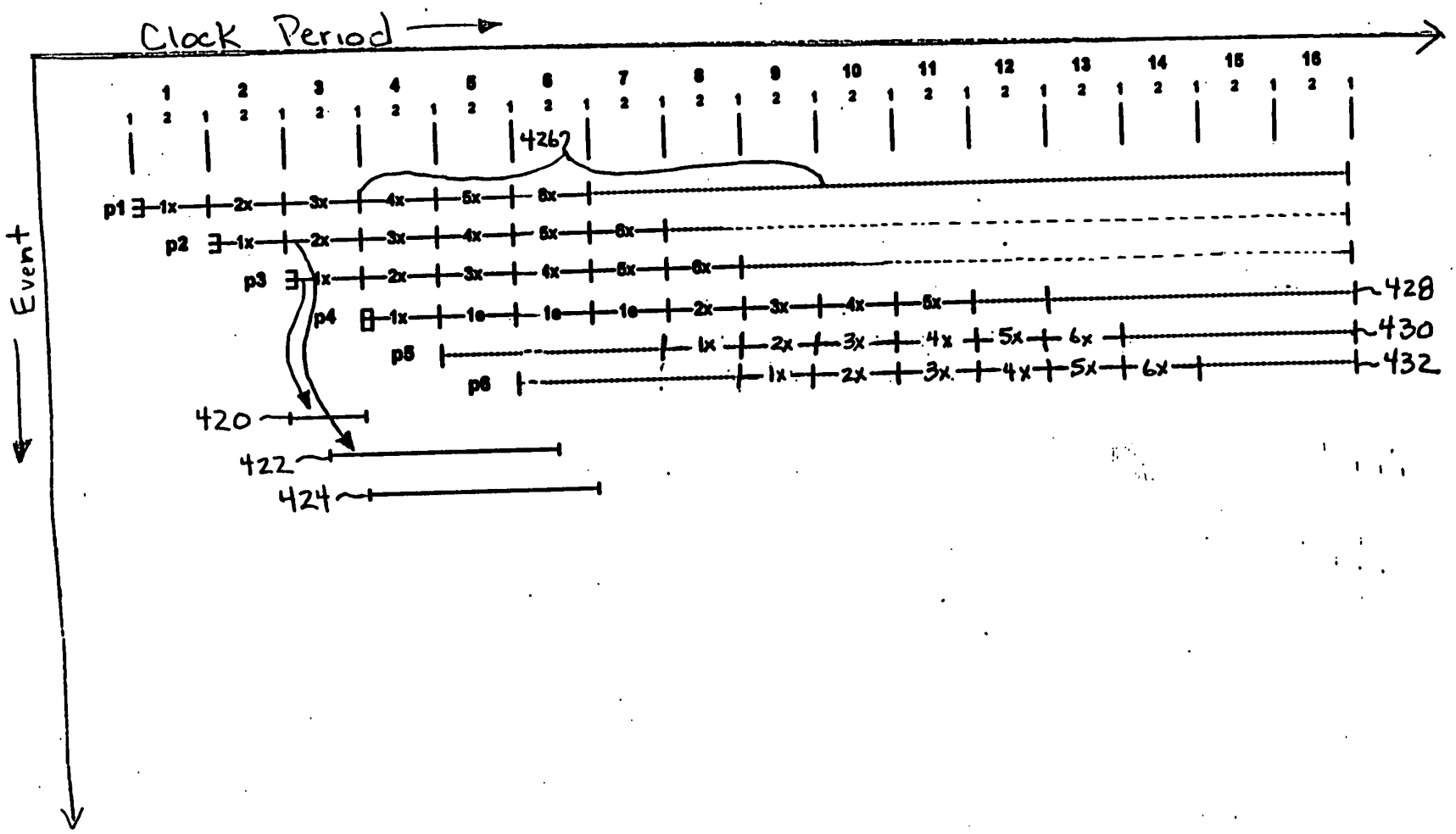

Clock Period
Event
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
426
p1
p2
p3
p4
p5
p6
1x 2x 3x 4x 5x 6x
428
430
432
420
422
424

Figure 17